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A Unified Analytical and Simulation Framework for Design of SiC MOSFET and Si IGBT High-Voltage Traction Inverters

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***Abstract*— This paper presents a unified analytical framework for comparing three inverter topologies for medium-power motor drives: a conventional two-level SiC MOSFET inverter, a three-level neutral-point - clamped silicon IGBT inverter (NPC), and a three-level T-type (T-NPC) silicon IGBT inverter. The device models were parameterized using the manufacturer's datasheet characteristics and validated through detailed PLECS simulation models for railway traction drive systems. PLECS-based validation is commonly employed during the design and optimization stages of industrial power electronic systems prior to the prototype development and hardware testing. The framework combines electrothermal device models, topology-dependent loss equations, an equivalent RLC motor model, and standardized thermal networks with equal output power. A 33 kW PMSM drive supplied from a 2500 V DC bus is analyzed using PLECS simulations at 5, 10, 20 and 40 kHz switching frequencies to assess electrical and thermal performance. Both analytical results and simulations clearly demonstrate that the SiC MOSFET offers an inherent advantage for medium- to very high power applications, especially where superior thermal performance in a compact form factor is critical.**

Keywords - SiC MOSFET, Three-level NPC inverter, T-type inverter, Traction Inverters, Switching losses, Thermal analysis, PLECS

I. Introduction

Power electronic converters are essential in modern electric drive systems for industrial automation, transportation, renewable energy, and railway applications. Voltage source inverters (VSIs) are widely used to control AC machines such as induction motors and permanent magnet synchronous motors (PMSMs). Increasing demands for efficiency, power density, and reliability are driving the development of advanced inverter topologies and semiconductor devices [1]. Conventional two-level (2L) silicon IGBT inverters are widely used in medium- and high-power applications due to their simple structure and control [2]. However, increasing DC-link voltages, such as the 2500 V commonly used in railway traction systems, require higher voltage-rated switching devices and motivate the adoption of multilevel topologies [3]. Among these, three-level Neutral Point Clamped (NPC) and T-type NPC (T-NPC) inverters are widely employed. NPC inverters reduce device voltage stress and improve output waveform quality through clamping diodes [4], while T-NPC inverters replace these diodes with active switches to reduce conduction losses and improve efficiency [5] [6] [7]. In parallel, wide-band gap devices, such as SiC MOSFETs, offer lower switching losses, higher breakdown voltages, and faster switching speeds than conventional silicon devices [3]. This paper compares a 2L SiC MOSFET inverter, a 3L NPC Si-IGBT inverter, and a 3L T-NPC Si-IGBT inverter using an analytical framework that evaluates efficiency, size, and complexity to identify the most suitable topology.

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II. System Description

The system framework for comparing the three inverter topologies is shown in Figure 1. The standard two-level inverter is composed of six power switches arranged in a three-phase bridge structure. Each phase leg includes a pair of complementary switches that produce two distinct voltage levels at the output. In this study, SiC MOSFETs are employed in the two-level inverter because their high switching speed and low switching losses support the operation at elevated switching frequencies. [2].

The three-level NPC inverter reduces device voltage stress and improves output waveform quality through multilevel voltage generation. The T-type inverter replaces the clamping diodes with active switches, reducing conduction losses and providing higher efficiency while maintaining the advantages of the NPC topology. [5] [8] [3] [9].

The LC filter is used to remove switching harmonics from the load current. The 3-phase motor is represented by Resistor-Inductor ($L_L R_L$) load. The inductor (L_L) represents the self-inductance of the motor winding and the resistance R_L represents the power delivered to the load [10].

A. Operating Conditions

The performance of the proposed inverter topologies is assessed in PLECS using identical operating conditions. The inverter is rated at 33 kW output power with a power factor of 0.8. The DC-link voltage is fixed at 2500 V and sinusoidal pulse-width modulation (SPWM) is applied for the switching control. The inverter runs at an output frequency of 50 Hz and supplies a line-to-line RMS output voltage of 1.38 kV. Under these conditions, the RMS phase current is about 17.3 A. The configuration results in an output voltage of 1380 Vrms and an output current of 17.3 Arms. All inverter topologies operate under identical conditions to allow for a fair comparison of their efficiency, power losses, and thermal behavior. For all inverter topologies considered in this study, employ Sinusoidal Pulse Width Modulation (SPWM) to ensure a consistent comparison framework and observed performance differences primarily attributed to the inverter topology and semiconductor devices rather than modulation-related effects.

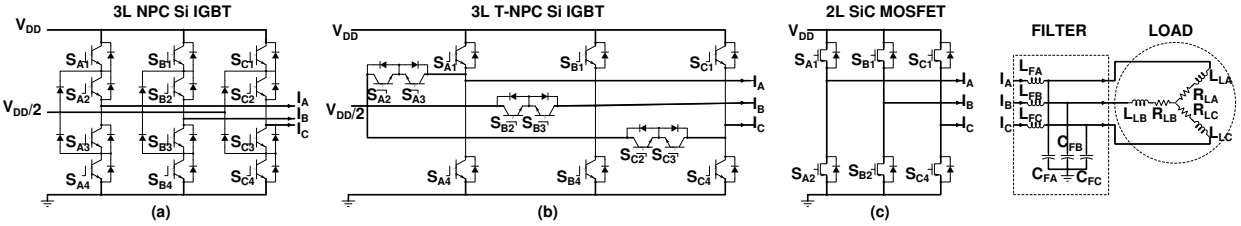

Fig. 1. System description: Inverter Topology [(a) three-level NPC, (b) three-level T-NPC, and (c) two-level with SiC MOSFET followed by LC current filter and the load

III. Electrical Performance

Power loss analysis is performed to evaluate the efficiency and thermal performance of the inverter topologies investigated under identical operating conditions. Total inverter losses comprise semiconductor conduction and switching losses. Analytical calculations are based on datasheet parameters of the Microchip MSCO25SMA330B4N SiC MOSFET [11] and Semikron SKM100GAL17E4 Si-IGBT module [12], while simulation results are obtained using detailed PLECS models. The analysis covers switching frequencies from 5 to 40 kHz, and Table-I compares analytical and simulated losses. Close agreement validates the proposed loss model. The results show that switching losses dominate at higher frequencies; the 3L T-NPC inverter exhibits slightly lower losses than the 3L NPC inverter, while the 2L SiC MOSFET inverter achieves the lowest total losses across the entire frequency range due to the superior switching performance of SiC devices. Although SiC MOSFETs are capable of operating efficiently at switching frequencies exceeding 100 kHz, the frequency range considered in this study was selected to reflect the practical operating conditions of medium-voltage railway traction drives. In such applications, the switching frequency is typically limited by efficiency requirements, thermal constraints, EMI considerations, and machine-related factors, rather than the capability of the semiconductor device alone. Therefore, the investigated frequency range provides a realistic basis for comparing Si-based and SiC-based inverter technologies in railway traction systems.

Figure 2 illustrates how efficiency varies with the switching frequency for the different inverter topologies. It is evident from Table I that efficiency decreases as the switching frequency increases, which is attributed to higher switching losses. The 2-level SiC MOSFET inverter consistently exhibits markedly higher efficiency than the 3-level NPC and T-NPC inverters, especially at elevated switching frequencies.

Device losses consist of conduction and switching losses. The IGBT conduction loss model used the dynamic on-resistance $R_{on(IGBT)}$ and the zero on-state voltage: $P_{con(IGBT)} = V_0 I_{av} + R_{on(IGBT)} I^2_{rms}$, where I_{av} and I_{rms} are the average currents of the device and rms. For SiC MOSFETs, conduction losses were $P_{con(MOS)} = R_{DS(on)} I^2_{rms}$, based on *ON* resistance $R_{DS(on)}$. Switching losses can be expressed as: $P_{sw} = f_{sw} 1/T \int (E_{on} + E_{off}) dt$ where E_{on} and E_{off} are the energy dissipated by the device during the switching transition. Detailed analysis of the specific topologies can be found in [13] [14] [15].

TABLE I
Calculated and Simulated Loss for all three inverters

3L NPC	**Calculated Loss (W)**			**Simulated Loss (W)**		
f_{sw}	**Cond.**	**Switch.**	**Total**	**Cond.**	**Switch.**	**Total**
5 kHz	96	150	246	91	150	241
10 kHz	96	299	395	93	316	409
20 kHz	96	600	696	96	696	792
40 kHz	96	1200	1296	98	1390	1488
3L T-NPC						
5 kHz	77	162	239	79	162	241
10 kHz	77	335	412	80	341	421
20 kHz	77	750	827	83	752	835
40 kHz	77	1860	1937	81	1862	1943
2L SiC						
5 kHz	25	42	67	26	42	88
10 kHz	25	84	109	26	84	110
20 kHz	25	170	195	27	171	198
40 kHz	25	350	375	29	352	381

Cond.: Conduction loss; **Switch.**: Switching loss; f_{sw}: switching freq.

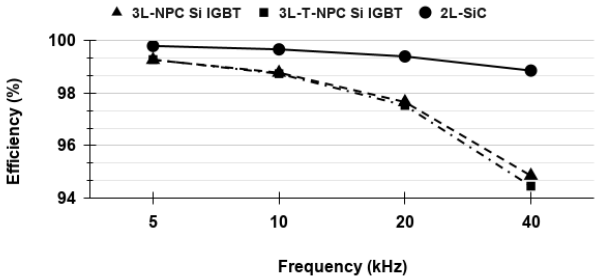

Fig. 2. Efficiency vs. Switching Frequency for three inverters

IV. Filter Design

An LC output filter was designed to attenuate switching harmonics and provide smooth current to the PMSM load. The filter inductance (L_f) was selected to limit the inverter ripple current to approximately 10% of the peak current using the relation $L_f = V_{DC}/(8\Delta I_{OUT} f_S)$ where ΔI_{OUT} is the output ripple current [16]. The capacitance (C_f) was then calculated from the LC resonance condition, with the cutoff frequency set to $f_c = f_{sw}/10$. The filter parameters resulting for the two-level SiC MOSFET inverter and the three-level NPC Si IGBT inverter at 5, 10, 20 and 40 kHz are listed in

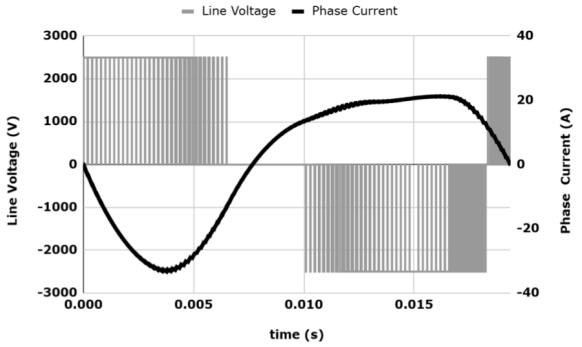

Fig. 3. PLECS time-domain simulation for 2L SiC inverter

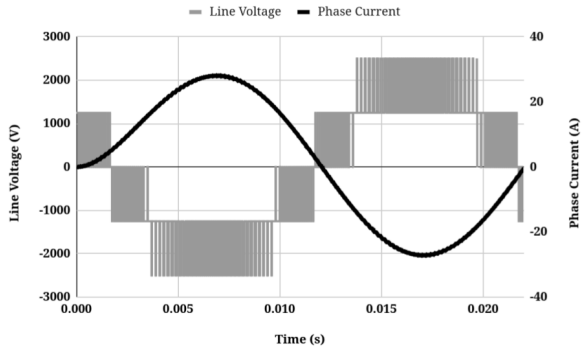

Fig. 4. PLECS time-domain simulation for 3L NPC inverter

Table II. Higher switching frequencies reduce the required inductance and capacitance because of a lower current ripple. In addition, the NPC topology produces smaller voltage steps than the two-level inverter, reducing current ripple and filter size; specifically, the three-level NPC requires a smaller inductance since the applied voltage step is $V_{DC}/2$.

The *filter volume* can be calculated using the *area-product* approach for the inductor and *capacitor-constant* approach for the capacitor [16]. The inductor volume can be expressed as $Vol(L_f) = k_L K_o L_f^{6/7}$ where k_L is a weak function of f_s and can be approximated to $k_L \approx 20$ and K_o approximated to $K_o \approx 10 cm^3/mH^{6/7}$ based on empirical data in [16] and is a function of physical parameters including the ratio of iron loss to copper loss, maximum flux density, current waveform factor, maximum temperature rise.

The volume of the filter capacitor C_f is calculated using the expression $Vol(C_f) = k_c C_f V_{nom}^2$ where V_{nom} is the nominal voltage of the capacitor and k_c is the constant volume of the capacitor. For our comparative calculation, we use $k_c = 72\ cm^3/V^2F$ which was derived in [16] as the minimum notice for different types of X2 type of capacitors. The total volume is calculated by adding both volumes and is tabulated in Table II.

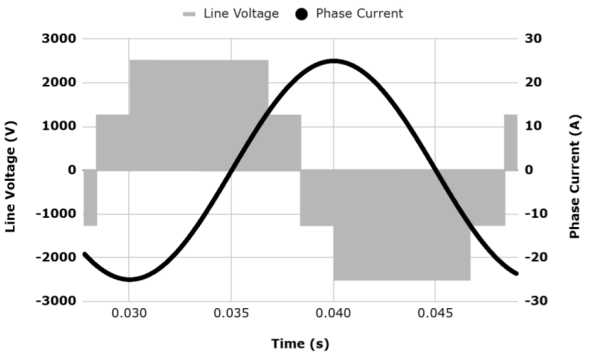

Fig. 5. PLECS time-domain simulation for 3L T-NPC inverter

TABLE II
FILTER SIZE VS. SWITCHING FREQUENCY

Topology	f_{sw} (kHz)	L_f (mH)	C_f (μF)	Vol-L_f (cm^3)	Vol-C_f (cm^3)
2L SiC	5	8	127	1,188	57,150
	10	4	63	656	28,350
	20	2	32	362	14,400
	40	1	16	200	7,200
3L NPC	5	4	254	656	114,300
	10	2	127	362	57,150
	20	1	64	200	28,800
	40	0.5	32	110	14,400
3L T-NPC	5	4	255	656	114,750
	10	2	127	362	57,150
	20	2	64	362	28,800
	40	0.5	32	110	14,400

Harmonic Performance Comparison: The FFT results indicate that the 3L NPC and T-NPC inverters produce a significantly lower harmonic distortion than the 2L SiC inverter due to their multilevel voltage waveforms and reduced current ripple. Across the switching frequency range of 5-40 kHz, the 2L SiC inverter exhibited THD values of 0.27 to 0.29, while the 3L T-NPC inverter maintained approximately 0.1050 THD. The 3L NPC inverter exhibited THD decreasing from 0.04 to 0.01. Although the harmonic power of 2L SiC topology is higher than that of 3L topologies, the 2L SiC topology can be operated at a much higher frequency resulting in a smaller filter size.

V. THERMAL PERFORMANCE

Thermal modeling is an essential and integral part of accurately modeling power systems. The PLECS simulator allows you to enter the switching energy from the datasheet along with thermal resistance. This allows for real-time thermal profiles. For this work, in order to assess the heat sink size for each topology, the ambient temperature was set so that the junction temperature reached it's maximum value and then using the model shown in Figure 6, the heat sink volume was calculated [17] [16].

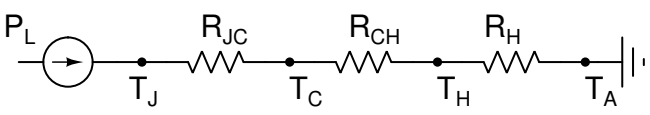

Fig. 6. Thermal model

Heat-sink volume: The thermal network of the switching device is shown in Figure 6. T_J, T_C, T_H, T_A denote the

junction, the case, the heat sink and the ambient temperatures, respectively, and R_{JC}, R_{CH}, R_H are the thermal resistances of the junction-to-case, the case-to-heat sink and the heat sink, where $R_H = (T_H - T_A)/P_L$. The heat sink volume analysis used the power losses of three systems at maximum output power and maximum junction temperature ($T_{J-max} = 175°C$ for the SiC MOSFET and $T_{J-max} = 150°C$ for the Si IGBT). The calculated value of R_H allows the volume of the heat sink to be determined under natural convection. The fitting relation for the volume of various extruded, naturally cooled heat sinks at a specified R_H is given in [16] as:

$$Vol_{heatsink} = 3263\ e^{-13.09 \cdot R_H} + 1756\ e^{-1.698 \cdot R_H} \quad (1)$$

TABLE III
HEAT SINK VOLUME VS. FREQUENCY

f_{sw}(kHz)	Loss (W)	$T_H(°C)$	$R_H(°C/W)$	$Vol(cm^3)$
2L SiC	($T_J = 175°C$)			
5	67	166	1.58	121
10	110	159	0.90	383
20	198	148	0.44	836
40	381	120	0.16	1761
3L NPC	($T_J = 150°C$)			
5	240	142	0.34	1020
10	407	118	0.14	1884
20	791	64	0.01	4795
40	1794	25	-0.02	cooling
3L T-NPC	($T_J = 150°C$)			
5	241	142	0.34	1023
10	421	118	0.14	1926
20	835	59	0.00	cooling
40	1944	25	-0.02	cooling

$T_A = 60°C$

Table III shows the heat sink volume calculations for three inverters as a function of the switching frequency f_{SW}. An ambient temperature of $60°C$ was selected based on the *on-board equipment* specifications [17] [13].

From the table, it is evident that the SiC MOSFET offers a distinct thermal advantage over the Silicon IGBT in three-level topologies. For a specific switching frequency, for example $f_{SW} = 5\ kHz$, the difference in form factor is approximately 8.5. It is also apparent that the Si IGBT requires forced-air or liquid cooling at higher frequencies, whereas the SiC MOSFET can continue to operate using only natural convection cooling across the entire range of simulated frequencies.

VI. COMPARISON

In addition to the electro-thermal performance parameters, there are two additional parameters that become key factors when designing medium to high-power traction inverters.

Assembly complexity: The many devices and high-current paths increase design complexity and overall cost of the system. Gate driver count also scales with device number: a 2L SiC topology uses 6 switches; a 3L NPC uses 12 switches plus 6 neutral-point diodes; and a 3L T-NPC uses 12 switches [5] [18] [19]

Control complexity: Three main methods control the fundamental voltage generated by the three-level inverter to the load: 1) carrier-based PWM; 2) space vector modulation (SVM); and 3) selective harmonic elimination (SHE). The increased number of devices increases the complexity of the system [20]. A practical consideration associated with three-level NPC and T-NPC topologies is the maintenance of neutral-point voltage balance across the DC-link capacitors. Unequal capacitor voltages can lead to increased device voltage stress, waveform distortion, and reduced performance. Hence capacitor voltage balancing is required particularly under transient operating conditions and unequal loading scenarios. Furthermore, the sizing and monitoring requirements of the DC-link capacitor may be more demanding than those of a conventional two-level inverter. These factors contribute to the higher implementation and control complexity of three-level topologies.

TABLE IV
COMPARISON TABLE

	$f_{SW}(kHz)$	**2L SiC**	**3L NPC**	**3L T-NPC**
Switching Loss (W)	5 kHz	42	150	162
	40 kHz	352	1390	1862
Cond. Loss (W)	5 kHz	26	91	79
Current Harmonics		high	low	low
Filter Volume	5 kHz	1,315	910	911
(cm^3)	40 kHz	216	142	142
Heat sink Vol.	5 kHz	121	1020	1023
(cm^3)	40 kHz	1761	cool	cool
No. of switches		6	18	12
No. of gate drivers		6	12	12
Control complexity		low	high	high

VII. CONCLUSION

We applied this analytical and simulation framework to three high-voltage traction inverter topologies. Table IV presents results designers can use to select a topology before hardware implementation, significantly reducing design time. This work shows that SiC MOSFET switching losses are much lower than those of Si IGBTs at high switching frequencies (about five times lower at 40 kHz). As a result, a two-level SiC inverter can use a heat sink almost 8.5 times smaller than that of a three-level Si IGBT inverter operating at 5 kHz, which would otherwise need liquid or forced-air cooling at higher frequencies. Three-level converters need smaller filters than two-level converters at equal switching frequency, but two-level SiC MOSFET converters can switch much faster, also allowing smaller filters. The larger number of switching devices and gate drivers in three-level converters increases cost due to added assembly and control complexity. Although SiC-based inverters improve switching performance and efficiency, their faster switching can raise motor insulation stress from large dv/dt and increased EMI compared to three-level inverters. dv/dt stress and EMI will be analyzed in future work, along with experimental validation of the models.

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