A CONSTANT G_M RAIL-TO-RAIL OPAMP WITH A NOVEL INPUT STAGE FOR BICMOS PROCESS

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ABSTRACT

Abstract- A BiCMOS rail-to-rail operational amplifier capable of operating from supply voltages as low as 2.5V is presented. A new technique of achieving a rail-to-rail input common mode range using a bipolar input stage is developed. The new technique avoids the use of complementary pairs at the input and thus avoids complicated schemes for monitoring the constant g_m. The resulting variation of the g_m is within +/-5.64%. The output stage is also rail-to-rail with a class AB control providing 5ma of current to a 300 Ohm resistor in parallel with a $20pF$ load. The output stage can swing to within 50mV of each supply rail. The opamp was realized in a conventional 1.2μm BiCMOS process with a DC gain of 81dB and a unity gain frequency of 7.9 MHz.

Keywords: Operational Amplifier,input common mode range, g_m

1. INTRODUCTION

In the recent years, the need for operating circuits at low voltages has increased due to scaling of devices. The lowering of the supply voltage has an enormous impact on the signal handling capabilities of operational amplifiers. The dynamic range drastically decreases due to lower allowable signal voltages. In order to maximize the dynamic range the signal has to be as large as possible. This requires an output stage with rail-to-rail output voltage swing. The choice of the input stage depends on the application. In inverting feedback applications, an amplifier can be equipped with a conventional input stage, because the common-mode input range of the amplifier can be small for these types of applications. In non-inverting feedback applications, however, the common-mode input range swing can be as large as the signal itself. Therefore, an operational amplifier has to be equipped with a rail-to-rail input stage as well as rail-to-rail output stage in those applications. In the literature, a number of rail-to-rail architectures have been proposed recently. The key problem in designing an input stage lies in maintaining constant g_m(transconductance) all throughout the rail-to-rail input common mode range so that the unity-gain bandwidth, phase margin and slew rate are maintained approximately constant. This is very much necessary for power-optimal frequency compensation. For Bipolar and CMOS processes, constant g_m rail-to-rail input stages using complementary stages have been reported [1, 2, 3]. For BiCMOS process, constant g_m rail-to-rail input stages can also be designed using PMOS's and NMOS's. However, input stages using bipolar transistors may be preferable due to higher transconductance, which leads to an opamp that has a higher gain-bandwidth product. In this paper, a new constant g_m rail-to-rail input structure suitable for BiCMOS process is proposed.

The remainder of the paper is organized as follows: Section 2 describes the input stage. Section 3 describes the class-AB output stage. The overall topology of the opamp is discussed in Section 4 followed by the frequency compensation in Section 5. Section 6 covers the circuit realization, implementation and measurement results. Section 7 concludes the paper.

2. INPUT STAGE

The conventional way to obtain a rail-to-rail input common mode range operation is to place a N-channel differential pair in parallel with a P-channel differential pair. The draw back of complementary input stage is that the transconductance(g_m) changes by a factor of two within the common-mode input range, as shown in Figure 1. The variation of the g_m impedes optimal frequency compensation because the bandwidth of an operational amplifier is proportional to the g_m of its input stage. In order to obtain an optimal frequency compensation, the g_m of the input stage has to be constant [8]. There are several schemes proposed for maintaining constant g_m. From Figure 1 it can be seen that in order to obtain a constant g_m over the common-mode input range, the g_m at the lower and upper part of the common-mode input range has to be increased by a factor of two. Since the g_m of a MOS transistor operating in strong inversion is proportional to the square-root of its drain current, the tail current of the actual active input pair could be increased by a factor of four.

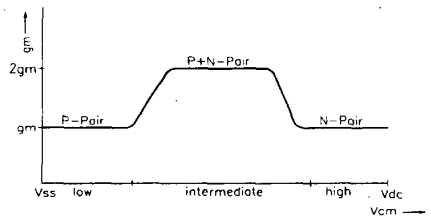

Figure 1: g_m versus the common-mode input voltage for the complementary input stage

The implementation of this scheme can be quite complex. And this scheme also requires that for a constant g_m the W over L ratios of the P-channel and N-channel input pair have to obey the following relation:

$$\frac{\mu_N}{\mu_P} = \frac{(\frac{W}{L})_P}{(\frac{W}{L})_N} \quad (1)$$

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If the ratio of μ_N over μ_P differs from its nominal value because of process variations, the g_m will also vary. For example if μ_N over μ_P changes about 10%, the variation in g_m will be approximately 10%.

The proposed input stage given in Figure 2 avoids all such complications. As shown in the figure, two NPN bipolar differential pairs(Q_0-Q_1 and Q_2-Q_3) are used to achieve rail-to-rail input common mode range. The differential pair(Q_2-Q_3) is conducting only for a limited range of input common mode voltage from near mid supply to positive rail. The other pair (Q_0-Q_1)is active

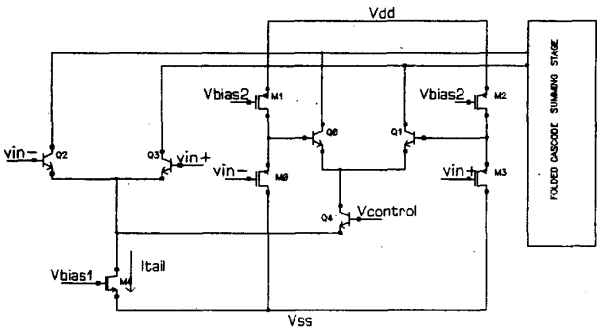


Figure 2: Proposed rail-to-rail input stage

for the remaining part of the range. A constant current is maintained during both the ranges of operation to hold the g_m constant. The current switch Q_4 with a bias $V_{control}$ sets the limit of operation. Since the total current flowing through both stages remains constant, so does the g_m of the input stage. When the input common mode voltage is near the negative rail, the tail current I_{tail} is steered into the differential pair(Q_0-Q_1). The input voltage needs to be shifted up to make the differential pair active. The level shifter(M_0-M_3) are used for this purpose. For the input common mode voltage equal to V_{ss}, the source-to-gate voltage of M_0 and M_3 have to satisfy the following condition.

$$V_{SG0} \geq V_{BE0} + V_{CEsat4} + V_{DSsat4} \quad (2)$$

The input common-mode voltage that turns off the Q_0-Q_1 differential pair is set by $V_{control}$, which has a minimum value equal to V_{BE2} + V_{DSsat4}. At this common mode voltage, the base voltages of Q_0 and Q_1 are equal to V_{BE2} + V_{DSsat4} + V_{BE0} + V_{CEsat4} + V_{DSsat4}. Since M_1 and M_2 have to remain in saturation, the minimum supply voltage can be determined as

$$V_{DDmin} = V_{BE2} + V_{DSsat4} + V_{BE0} + V_{CEsat4} + V_{DSsat4} + V_{SDsat1} \quad (3)$$

For typical values of V_{BE}(0.65V), V_{CEsat}(0.25V) and V_{DSsat} (0.15V), a minimum supply voltage of slightly more than 2V can be achieved.

The region of operation for which the two differential pairs Q_0-Q_1 and Q_2-Q_3 are active are given in equation (4) and (5). This is set by $V_{control}$.

$$Q_0 - Q_1 : V_{SS} < V_{CM} \leq V_{control} \quad (4)$$

$$Q_2 - Q_3 : V_{control} < V_{CM} \leq VDD \quad (5)$$

There is small region of overlap where both the pairs are active. However the g_m is still constant in this region since the total tail current of the differential pairs is constant.

In order to keep the g_m constant, the level shifter needs to have unity gain. In reality it is not unity and the gain of the level shifter is equal to

$$\frac{g_{mM0}}{g_{mM0} + g_{mbM0} + g_{dsM0} + g_{dsM1}} < 1. \quad (6)$$

Therefore, the g_m of the input pair also varies by the same factor. To operate the circuit with a supply voltage given by equation (3),

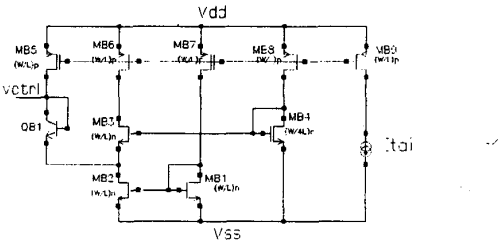


Figure 3: Bias circuit for the rail-to-rail input stage

$V_{control}$ needs to track $V_{BE2} + V_{DSsat4}$. A simple bias generator shown in Figure 3 is designed for this purpose. A standard configuration consisting of $M_{B1}, M_{B2}, M_{B3}, M_{B4}$ was used for generating V_{DSsat} across M_{B2}, which equals to V_{DSsat4} of Figure 2. I_{tail} is passed through Q_{B1} to give the required V_{BE} drop and hence, $V_{control}$ is equal to $V_{BE2} + V_{DSsat4}$.

The output currents of the input stage shown in Figure 2 are fed to a wide swing cascode load. A wide swing cascode load is used to boost the gain and at the same time maximize the swing.

3. CLASS AB OUTPUT STAGE

In order to efficiently use the supply power with high maximum output current with a low quiescent current, a class-AB output stage has been used. A compact class-AB output stage is shown in Figure 4. [6]. It consists of two common-source connected output transistors, M_{25} and M_{26}, which are directly driven by two-in-phase signal currents, I_{in1} and I_{in2}. The floating class-AB control is formed by M_{19} and M_{20}. The stacked diode-connected transistors, $M_{23} - M_{24}$ and $M_{21} - M_{22}$ bias the gates of the class-AB transistors M_{19} and M_{20} respectively. The minimum supply voltage is limited by the demand for a fully rail-to-rail common mode input range. Therefore, two stacked gate-source voltages are allowed in the class-AB output stage. The floating class-AB control transistors, the stacked diode-connected transistors and the output transistors set up two translinear loops M_{19}, M_{21}, M_{22}, M_{25} and M_{20},M_{23}, M_{24}, M_{26} which determine the quiescent current in the output transistors. The class-AB action is performed by keeping the voltage between the gates of the output transistors constant. Suppose the in-phase signal current sources I_{in1} and I_{in2} are pushed into the class-AB output stage, the current of the P-channel class-AB transistor M_{20}, increases while the current in the N-channel class-AB transistors, M_{19}, decreases by the same amount. Consequently, the gate-voltages of both the output transistors move up. Thus the output stage pulls a current from the output node. This action continues until the current through the

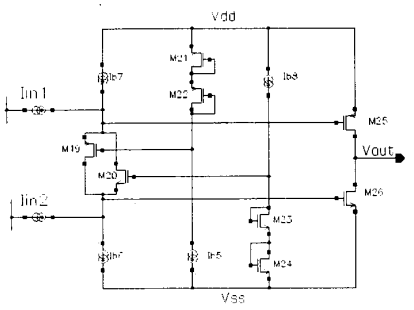


Figure 4: Floating class AB control

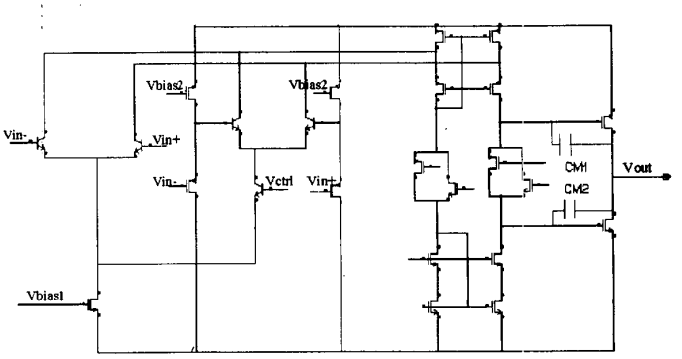


Figure 5: Overall design of the rail-to-rail operational amplifier($V_{control}$ bias circuit is not shown for simplicity)

P-channel class-AB transistor is equal to I_{b7}. Now, the current of the P-channel output transistor is kept at minimum value, which can be set by W/L ratio of the class-AB control transistors. Note that the current through the N-channel output transistor is still able to increase. A similar discussion can be held when an input signal is pulled from the class-AB output stage.

4. TOPOLOGY OF THE OPAMP

In the previous sections, the rail-to-rail input stage and the rail-to-rail class-AB output stage have been described. In this section the overall topology of the operational amplifier will be described.

The conventional way to design a two-stage opamp is to place the input stage, $Q_0 - Q_3$, the folded cascode summing stage and the class-AB stage in cascade. But this approach has some significant drawbacks. Firstly the gain of the opamp decreases because the bias current sources of the class-AB control, I_{b6} and I_{b7}, are in parallel with the cascode transistors of the summing circuit. Secondly, apart from the input transistors, $Q_0 - Q_3$ and the current sources of the summing circuit, the bias current sources of the class-AB control, I_{b6} and I_{b7}, also contribute to the noise and offset of the amplifier.

One way to overcome the above drawbacks is to add an intermediate stage. But adding the intermediate stage will increase the die area and also it makes the frequency compensation difficult. An alternative way to reduce the noise and offset contribution of class-AB control without the additional cost of die area or loss of unity gain frequency, is to shift the floating class-AB control, M_{19} and M_{20}, into the summing circuit as shown in Figure 5. The floating class-AB control is biased by the cascodes of the summing circuit[7]. The class-AB control and therefore the quiescent current in the output transistors, suffers from supply voltage variations. To make the quiescent current of the output transistors insensitive to supply voltage variations, the floating current source should have the same supply voltage dependency as the class-AB control. As described in [6] by biasing the current mirrors with the floating current source which has the same architecture as the class-AB control the variation in the quiescent current can be minimized.

5. FREQUENCY COMPENSATION

Using the topology as described in the previous section, a compact opamp with miller compensation has been designed, and is shown in Figure 5. The opamp consists of rail-to-rail input stage $Q_0 - Q_3$, a summing circuit and a rail-to-rail class-AB output stage $M_{19} - M_{26}$. The opamp is compensated using the conventional Miller technique. The capacitors C_{M1} and C_{M2} around the output transistors, M_{25} and M_{28}, split apart the poles ensuring a $20dB$ per decade roll off of the amplitude characteristic. The Conventional Miller splitting shifts the output pole to a frequency of approximately

$$\omega_{out} = \frac{g_{m0}}{C_L} \tag{7}$$

where g_{m0} is the transconductance of the output transistors and C_L is the load capacitor. The unity gain frequency of the opamp is approximately given by $\frac{g_{m0}}{C_{M1}+C_{M2}}$.

6. REALIZATION AND MEASUREMENT RESULTS

The opamp has been realized in 1.2μm BiCMOS process. The N-channel transistors and P-channel transistors have threshold voltages of 0.69V and -0.97V respectively. The micrography of the compact opamp with Miller compensation is shown in Figure 6.

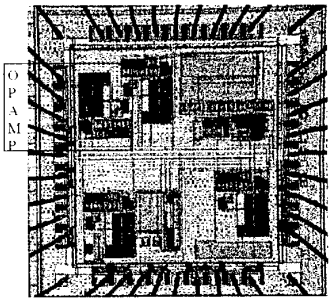
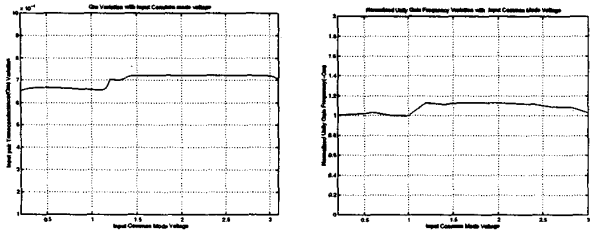


Figure 6: Die Photograph of the Rail-to-Rail Opamp

The opamp has a unity-gain bandwidth of 7.9MHz, with a load of $20pF$ and 300Ω resistor. The unity gain phase margin is 64°.

Simulation result shows that the variation of input pair g_m with input common mode voltage is around +/-5.2% as shown



(a) (b)

Figure 7: (a)Simulated input pair Gm variation with the input common mode voltage (b) Unity gain frequency variation with the input common mode voltage on silicon

in Figure 7(a).This includes the g_m variation due to the tail current variation of NMOS current source and level shifter non-unity gain. Figure 7(b) shows the experimental result of variation of unity gain frequency with input common mode voltage. Over the common-mode range the unity gain frequency varies by +/-5.64% only. Since the unity gain frequency is proportional to g_m of the input pair it can be concluded that the g_m of the input pair approximately varies by +/-5.64% only. Figure 8 shows small signal

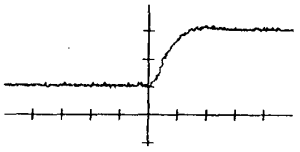


Figure 8: Small signal input step response. x-axis scale = $200ns$ y-axis scale = $50mV$

step response of the opamp. The opamp responds to small signals within 1% of the final value in $332ns$, for a load of $20pF$ and a step of $100mV$. The 1% settling time of the large-signal is $830ns$, for a capacitive load of $20pF$ and 300Ω and a step of 1V as shown in Figure 9. From Figure 8 it can be seen that the slew-rate of the

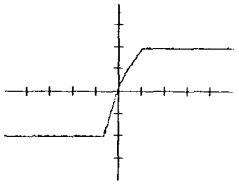


Figure 9: Large signal input step response. x-axis scale = $500ns$ y-axis scale = $200mV$

opamp is $2V/\mu s$. This slew rate changes with the common mode voltage.

The minimum supply voltage is 2.5V. At this voltage the opamp dissipates only $2.25mW$. At a supply voltage of 2.5V to 3.3V the opamp is able to deal with rail-to-rail input common-mode voltages. The opamp has a rail-to-rail output swing. The gain of the opamp is $81dB$.

Active Area	$0.16mm^2$
Supply Voltage Range	2.5V - 6V
Peak Output Current	5 mA
Common-mode Input Range	V_{ss}-0.2 to V_{DD}+0.2
Output Voltage Swing	V_{ss}+0.2 to V_{DD}-0.07
Open Loop Gain	81 dB
Unity Gain Frequency	7.9 MHz
Phase Margin	64°
Slew rate(at mid rail input common mode)	2 $V/\mu S$
Large signal settling time(1%) V_{step}= 1V	830 ns
Small signal settling time(1%) V_{step}= 0.1V	332 ns

Table 1: MEASUREMENT RESULTS Vsupply=3.3V, Rload = 300Ω, Cload = 20 pF, TA = 27 °C

7. CONCLUSION

A two stage BiCMOS operational amplifier with a novel rail-to-rail input stage and output stage has been presented. Experimental results shows that the g_m of the input stage varies by only +/-5.64% over the common-mode input range, mainly due to the variation of the gain of the level shifter and the output current of the tail current source.

Performance of this simple design is comparable with performance of the design in [3, 4, 5] without any complicated schemes for g_m control. However input offset voltage may vary with the common mode even though it is small.

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