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Design of 1 V Switched-Current Cells in Standard CMOS Process

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Abstract

The minimum supply voltage for a typical switched-current (SI) cell can be shown to be greater than $2V_T + 2V_{DSsat}$ approximately due to the fact that an additional voltage drop is required for the MOS switch, which is connected to the gate of the memory transistor. Thus, a minimum supply voltage of 1.5 V is usually required in a standard CMOS process. In this paper, an active switching scheme is proposed for designing SI cells. The minimum supply voltage is equal to $V_T + 2V_{DSsat}$. As a result, 1 V SI cells that exhibit low charge injection errors can be achieved.

1. Introduction

Low voltage and low power circuit design is increasingly important due to the demands in battery-operated systems and wireless communication systems. In addition, advances in CMOS process also drive down the supply voltage due to the reliability issues associated with these processes. In the near future, supply voltage will be reduced down to 1 – 1.5 V. However, the threshold voltages of the devices in these processes do not scale down at the same rate as the supply voltages. As a result, it presents a great challenge in the design of analog circuits unless enhancements on the standard CMOS process (e.g., with low-V_T option [1]) are used. However, these enhancements usually lead to the increase of overall cost. Since switched-current (SI) technique is an important analog signal processing technique, in this paper, we will focus on the design of SI cells, which not only can operate at low voltage (1 V) but also can provide high accuracy and high speed of operation.

2. Conventional SI cells

Over the years, many elegant SI cells have been proposed [2]. However, the minimum supply voltage for conventional SI cells can be understood from the basic first generation SI cell as shown in Figure 1. The switch S_1 is usually realized using NMOS that requires a voltage of $V_{TNS1} + V_{OV}$ to turn it on where V_{OV} is the minimum required overdrive voltage to satisfy the settling time requirement when the SI cell is in track mode. Therefore, the minimum supply voltage $\min\{V_{DD}\}$ can be written as

$$\min\{V_{DD}\} = V_{TN2} + V_{DSsat2} + V_{TNS1} + V_{OV} \quad (1)$$

where V_{DSsat2} is assumed to be the maximum required excess bias voltage of the memory transistor M_2 when the input signal is at its maximum. If V_{OV} is approximately equal to V_{DSsat2}, $\min\{V_{DD}\}$ will be approximately equal to $2V_{TN} + 2V_{DSsat}$. For conventional CMOS process, V_{TN} is usually above 0.5 V. Therefore, $\min\{V_{DD}\}$ will be about 1.5 V as reported in the literature [3]. This argument is usually true for most SI cells since a switch is normally connected to the gate of the memory transistor. If PMOS is used for S_1 and $V_{TN2} + V_{DSsat2}$ is greater than $|V_{TP}| + V_{OV}$, then $\min\{V_{DD}\}$ will be equal to $V_{TN2} + V_{DSsat2} + V_{SDsat3}$.

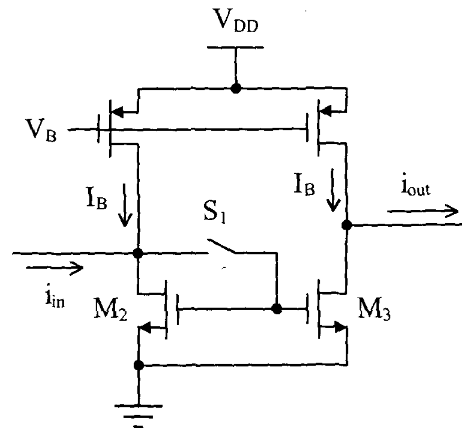

Figure 1: Basic first generation SI cell

Hence, a supply voltage of 1 V can be achieved. However, these conditions cannot be satisfied in conventional CMOS process and the overdrive voltage may not be sufficiently large due to body effects and process variations. The same conclusion can be drawn when S_1 is a NMOS and M_2 is a PMOS.

3. Proposed SI cells

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To design low voltage SI cells, an active switching technique is proposed in this paper. A SI cell similar to the first generation cell is shown in Figure 2. During the track mode, the drain current of M_3 I_{D3} is assumed to be equal to I_B and I_{D1} is equal to $I_B + i_{in}$. Since M_2 is sized to operate in saturation region and is acting as common gate amplifier, it helps reducing the input impedance at the input node to $1/g_{m1}g_{m2}r_{ds3}$. Similar to other SI cells with common gate amplifier [4] [5], the conductance ratio error resulted from the non-ideal finite input and output conductance of the SI cell is reduced. When ϕ turns low, both M_2 and the current source M_3 are off. This is equivalent to turn of the common gate amplifier. As a consequence, the voltage at the gate of the memory transistor M_1 will remain unchanged ideally. The minimum supply voltage for this circuit is $\max\{V_{TN} + 2V_{DSsat}, 3V_{DSsat}\}$, which can be lower than 1 V for $V_{TN} < 0.7$ V. Since M_2 and M_3 are switched off from saturation region instead of from triode region, the charge injection error is different from conventional SI cells and is illustrated in Figure 3. During the track mode, the channels of M_2 and M_3 are pinched off and disconnected from the drain node. Therefore, there are almost no charges flowing to the drains when M_2 and M_3 turn off. Although the gate voltage of M_1 is not affected by the channel charge, it will be by two other effects: (1) clock feedthrough and (2) the difference in off time between M_2 and M_3 that produces a current, which charges the gate voltage of M_1 for a short period of time. Fortunately, not only the first effect is input signal independent but also the second one. Since the current flowing through both M_2 and M_3 is always fixed by the current source I_B, and the source voltage of M_2 is also fixed equal to $V_{DD} - V_{GS2}$ during track mode, the amount of current charging the gate voltage of M_1 will be the same when the difference in off time between M_2 and M_3 is the same in each clock cycle.

During track mode, the transfer function between i_{in} and the gate voltage of M_1 v_{g1} can be expressed as

$$\frac{v_{g1}}{i_{in}}(s) \approx \frac{g_{m2}C_1C_2}{s^2 + \left(g_{m2}/C_1\right)s + \frac{g_{m1}g_{m2}}{C_1C_2}}$$

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \qquad Q = \sqrt{\frac{g_{m1}C_1}{g_{m2}C_2}}$$

where $C_1=C_{sb2}+C_{db1}$ and $C_2=C_{gs1}+C_{db2}+C_{db3}$. To achieve a fast settling time, a large value of $g_{m1}g_{m2}/C_1C_2$ is required and the Q factor is required to be closed 0.707. The last condition can be obtained if g_{m2} is greater than g_{m1}. This is achieved by adding a fixed auxiliary current source can be added in parallel between the drain and the source of M_1 in Figure 2. This current source will reduce the biasing current flowing through M_1 and thus, reduces g_{m1}. However, a smaller g_{m1} will also lead to a smaller value of $g_{m1}g_{m2}/C_1C_2$. Thus, an optimization is required to obtain a short settling time. Furthermore, a higher value of V_{DD} also helps shorten the settling time in general since the transistors can have higher V_{DSsat}'s and hence, smaller capacitance due to smaller transistor sizes for a given input current range as well as transconductance. Another factor that is critical for fast settling is the turn on time of M_3. Since increasing the transconductance of M_B reduces the time constant at the gate of M_3, the biasing current I_B and the aspect ratio of M_B cannot be too small compared to I_{D3} and the aspect ratio of M_3.

The input impedance of the current cell can be shown to be

$$R_{in} \approx 1/\, g_{m1}g_{m2}r_{ds3}$$

As seen from the above expression, the input impedance is gm2rds3 times lower than the conventional current mirror. A simple resistor can be used for voltage-to-current conversion with very low harmonic distortion.

The non-ideal behavior of the transistor is mostly dominated by the V_T mismatch of the transistor. The second-harmonic (dominant) distortion and the gain error (σ_I/I) due to V_T mismatch can be shown to be

$$HD_2 \cong (A_{vT}/\ 8\ (WL)^{1/2}(V_{GS1}-V_{T1}))\times(i_{in}/i_{ref})$$

$$\sigma_I/I \cong 2A_{vT}/((WL)^{1/2}(V_{GS1}-V_{T1}))$$

where $A_{vT}/(W/L)^{1/2}$ is the standard deviation value for the V_T mismatch. The above mismatch effects can be greatly reduced by using a second-generation scheme as briefly discussed later.

The error on the output current due to clock feedthrough and difference in off time discussed above can be improved using a differential technique. However, the $\min\{V_{DD}\}$ is at least one extra voltage drop of a current source more. To minimize the supply voltage, a psuedo-differential technique is used. The resulting SI cell is shown in Figure 4 where two SI cells of Figure 2 are used. Since the charge injection errors on both SI cells are signal independent, they will be converted as common mode output current. This common mode current and the biasing current I_B are detected by M_9, M_{10} and M_{11} and then reproduced by M_{12} and M_{13} where the aspect ratios of M_9 and M_{10} are assumed to be one half of M_4 and M_8. Thus, in a first order approximation, i_{o+} and i_{o-} will only contain the differential signal.

To reduce the matching requirement and to obtain a more accurate output, the proposed cell can be extended to a second-generation structure. In this technique, a non-overlapping clock phase has to be used. During one phase, the input is sampled and in the other phase, the same sampling transistor is used to output the current. This will reduce the effect of the transistor mismatch but it will also reduce the sampling speed by twice the amount.

4. Simulation results

The proposed SI cells were design in a standard 0.25 μm CMOS process with $V_{TN} \approx 0.6$ V and $V_{TP} \approx -0.7$ V. Level-48 BSIM transistors model were used in HSPICE to simulate the design. A supply voltage of 1 V was used. Figure-5 shows the settling behavior of the proposed SI cell shown in Figure 4 during track mode. The input was assumed to be fully differential with a peak-to-peak value of 200μA and the biasing current I_B was set to 400μA. In order to simulate the worst case settling behavior, the SI cell was clocked from hold mode to track mode. At the same time a differential step input of 200uA was applied. As expected, the output current peaks before settling, showing a second order behavior as discussed. The peaking was due to the Q factor being greater than 0.707. The differential output current was settled to 0.1 % within 4.7ns. For sine wave input with a peak value of 200μA at a frequency of 3.2MHz, the simulation result is shown in Figure 6 in which a sampling rate of 100MS/s was used. The THD and the power dissipation were simulated to be 62dB and 1.64mW, respectively. For a sampling rate of 80MHz (input of 3.75 MHz) and 50MHz (input of 2.34 MHz) the THD was found to be 67dB and 68dB, respectively. As seen in Figure 6, the track mode consists of large spikes. These spikes are due to the second order behavior and also due to switching asymmetry. For THD calculation, the output current during the hold mode was used for spectral analysis. The output current values during the hold mode were written onto a file and then spectral analysis was done on the data using MATLAB.

5. Conclusion

In this paper, a low voltage (1 V) SI cell is proposed. The cell consists of a switched common gate amplifier. Since the transistors in the amplifier are pinched off during track mode, almost no channel charge will be flown to the gate of the memory transistor when the amplifier is switched off. As a result, all the charge injection is signal independent and hence, high accuracy can be achieved.

Reference:

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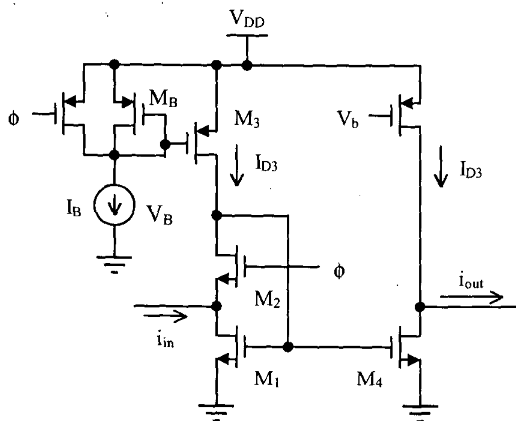

Figure 2: Proposed single-ended first generation SI

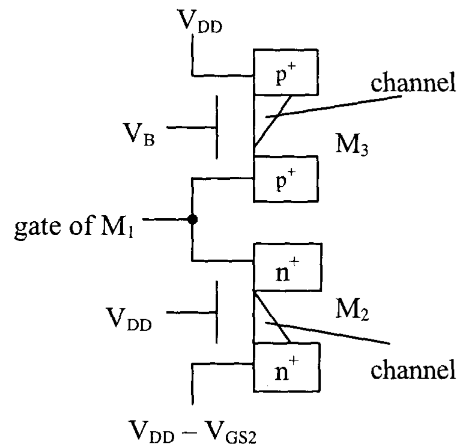

Figure 3: Channel charge distribution before the common gate amplifier turns off

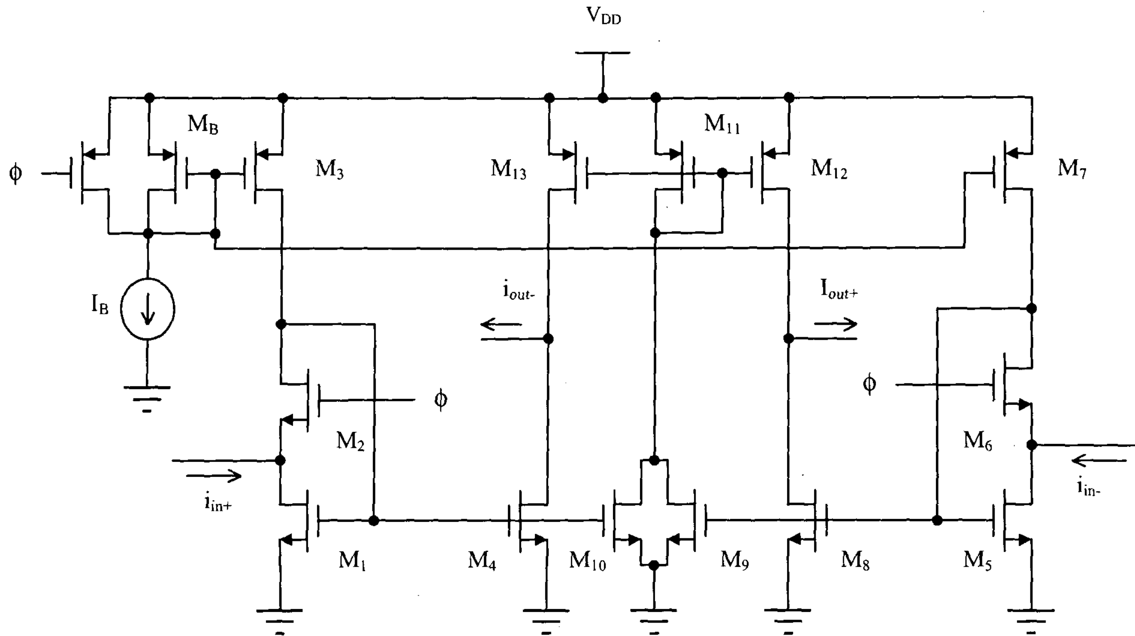

Figure 4: Proposed differential first generation SI cell

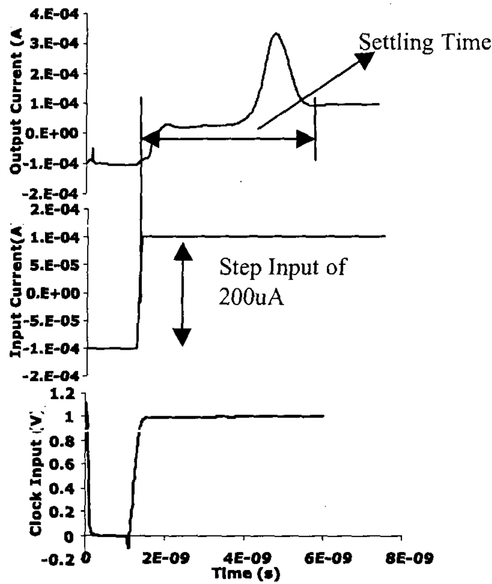

Figure 5: Settling behavior of the fully-differential SI cell for step input of 200μA

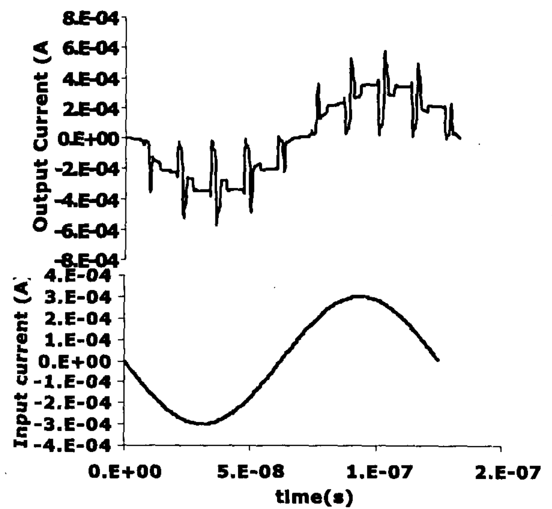

Figure 6: 300μA peak sine wave input is sample at 100 MS/sec.