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Simulations of Implant Epitaxy 4H-SiC MOSFET Designs for 1.5-1.9kV Power Electronics Applications

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***Abstract*— In this paper, we present simulation results of 1500V-1900V class 4H-SiC implantation and epitaxial MOSFET (IEMOSFET) structures. These structures are attractive due to the low doped epitaxial p-type layer which improves the channel mobility in the on-state, along with a high doped implanted layer to prevent punch-through and to give excellent off-state characteristics. In this work, a comparison of the IEMOSFETs with and without buried channel layers has been performed to obtain a trade-off between process complexity and device performance. Since interface traps can affect both device characteristics and long-term reliability, we performed a comparative study of the high trap density vs reduced trap density cases, where the low trap densities can be obtained using recently reported N2 annealing methods. We find that IEMSOFET without a buried channel leads to a on-resistance ($R_{DS(on)}$) of $50m\Omega$ in case of a channel length of $0.5\mu m$, compared to $75m\Omega$ with buried channel. The simulations show that $R_{DS(on)}$ drops from $112m\Omega$ to $75m\Omega$ by annealing N2. For the device without buried channel, the corresponding decrease in $R_{DS(on)}$,with N2 anneal, is from $55m\Omega$ to $50m\Omega$.**

Keywords- 4H-SiC, 1500V-1900V, IEMOSFET, With-buried channel, Without buried channel, Interface trap

I. Introduction

Silicon Carbide (SiC) power MOSFETs have emerged as a strong competitor to Si power devices in commercial power electronics applications due to their wide bandgap, high critical breakdown field, and superior thermal conductivity. SiC power devices are available in various voltage ratings from 600V to 3300V [1] [2]. The low on-resistance ($R_{DS(on)}$) and low turn-on and turn-off switching losses of these devices make them attractive for a range of applications, such as electric vehicles, industrial power systems, and railway propulsion systems [1] [2] [3]. In the literature on power devices, different device architectures have been proposed for SiC power MOSFETs, such as implantation-epitaxial MOSFETs and trench MOSFETs [4] [5] [6] [7], to reduce resistance. However, each advanced technology leads to increased fabrication complexity and cost. One of the main performance limiting factors in 4H-SiC MOSFETs is the low channel mobility due to the high interface trap density at the SiO2/4H-SiC interface [8]. These interface defects are generated due to interstitial carbon clusters, Si and C vacancies on the SiC surface, and oxygen vacancies on the oxide gate film [9]. The presence of charges trapped in such defects and the roughness of the oxide layer surface strongly influence the mobility of the channel carrier in high fields [9]. However, according to recent reports, trap densities can be reduced by thermal annealing in nitric oxide or POCl3 atmosphere [10] [11].

In this paper, we present the performance comparison of 4H-SiC power MOSFETs for different levels of interface trap densities from numerical modeling. We have chosen the implantation-epitaxial MOSFET architecture in which channel mobility is enhanced by a low-doped p-type epitaxial layer (above a high doped p-type implanted layer) to avoid implantation damage [4] [5] [6]. To reduce resistance, these devices have been reported with either a buried channel (BC) layer or a current spreading layer with $10^{17}cm^{-3}$ n-type doping. However, this introduces additional lithography and doping steps, complicating the CMOS-compatible fabrication flow. As industrial demand for 4H-SiC devices shifts toward cost-effective mass production, the overhead associated with buried channels must be weighed against the performance gains. Hence, we present a comparison of the device performance with and without buried channel layer in the 4H-SiC implantation-epitaxial MOSFETs (IEMOSFETs) to obtain a trade-off between the processing complexity and performance benefits along with the study of interface trap effects on their performance.

II. Device Structure and Simulation Environment

The 4H-SiC power MOSFETs of width $1000\ \mu m$ and channel length $0.5\ \mu m$ were simulated using the Silvaco TCAD tool (ATLAS Device Simulator). The total device is $10\mu m$ (one finger or lateral pitch). The drift layer is grown on an n-type substrate with a doping concentration of $10^{19}cm^{-3}$. The thickness of the drift layer is $22\mu m$ with n-type doping of $6\times10^{15}cm^{-3}$. The implanted p-well has a doping concentration of $3\times10^{18}cm^{-3}$ with a low doped p-type epitaxial layer with doping $5\times10^{15}cm^{-3}$ above it. The schematic diagrams of the device structures with and without the buried channel are shown in Fig.1. Both structures have an oxide thickness of $50\ nm$ with a p-well depth of $0.6\mu m$. The buried channel is created by $10^{17}cm^{-3}$ n-type doping above the p-type epitaxial layer in the structure shown in Fig.1. The doping of the source and the drain is $10^{19}cm^{-3}$ in both structures.

The device characteristics were simulated with different interface trap densities. The channel mobility model proposed by V. Uhnevionak et. al. [12] is considered for the on-

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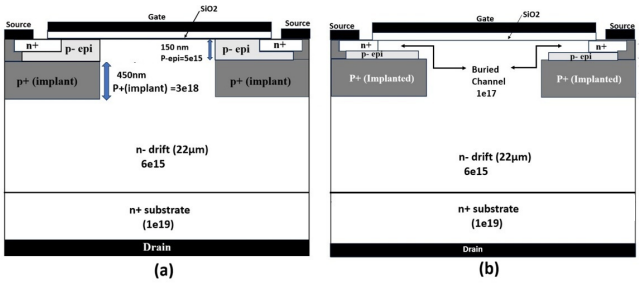

Fig. 1. Schematic diagram of 4H-SiC IEMOSFETs: (a)without and (b)with buried channel

state current simulations. This model calculates the channel mobility including the scattering effects caused by ionized impurities in the bulk (μ_{IMP}), the interface charges(μ_{IC}), surface roughness(μ_{SR}), surface phonons (μ_{SP}) and bulk phonons (μ_{BP}). The mobilities calculated due to each effect are combined by the Matthiessen rule to calculate the total mobility.

$$\frac{1}{\mu} = \frac{1}{\mu_{IMP}} + \frac{1}{\mu_{BP}} + \frac{1}{\mu_{IC}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_{SP}} \tag{1}$$

The first two mobility components of the above components, which together represent the bulk mobility μ_B:

$$\mu_B = \mu_{\min} T_N^{\alpha} + \frac{\mu_{BP1} T_N^{\xi} + \mu_{BP1} T_N^{\chi} + \mu_{BP1} T_N^{\alpha}}{1 + T_N^{\vartheta} \left(\frac{N_A}{N_{\text{ref}}}^{z}\right)} \tag{2}$$

Here $T_N = T/300\ K$ is the normalized temperature, $\mu_{\min}$ is the minimum value of the bulk mobility at 300 K and $N_{\text{ref}}, \alpha, \xi, \chi, \vartheta, z$ are the fitting parameters. μ_{BP1} and μ_{BP2} are two terms related to the bulk phonon. The values of the model parameters for the 4H-SiC MOSFETs are as per [12].

The mobility degradation due to Coulomb scattering at the interface trapped charges is represented by:

$$\mu_{IC} = \frac{\mu_1 T_N^{\nu} \left\{1 + \left[\frac{c}{c_{\text{trans}} \left(\frac{N_c}{N_0}\right)^{\eta_1}}\right]\right\}^{\nu}}{\left(\frac{N_c}{N_0}\right)^{\eta_2} D(x) f(E_\perp)} \tag{3}$$

Where μ_1 is a fitting parameter, c represents the electron concentration near the interface, N_c is the density of the interface trap, x is the distance from the interface and the perpendicular electric field to the oxide/4H-SiC interface is indicated as $E_\perp$. The parameter c_{trans} represents the screening of carriers in the inversion layer.

The functions $D(x)$ and $f(E_\perp)$ are given as

$$D(x) = e^{-x/l_{\text{crit}}} \tag{4}$$

$$f(E_\perp) = 1 - e^{-\left(\frac{E_\perp}{E_0}\right)^{\gamma}} \tag{5}$$

The mobility contributions resulting from surface roughness scattering and surface phonon scattering are modeled as follows:

$$\mu_{SR} = \left\{ \left(\frac{E_\perp}{E_{\text{ref}}}\right)^2 \frac{1}{\delta} + \frac{E_\perp^3}{\eta} \right\}^{-1} \frac{1}{D} \tag{6}$$

$$\mu_{SP} = \left\{ \frac{B}{E_\perp} + \frac{C(N_A)^{\alpha_1}}{E_\perp^{1/3} T} \right\}^{-1} \frac{1}{D} \tag{7}$$

The default values of the above model parameters for 4H-SiC have been assumed as per [12]. The mobility of the carrier in the drift layer has been evaluated according to the model proposed by Klaassen [13] which has been shown to provide an excellent match to the measured data [3]. For simulation of the off-state breakdown voltage, the model specifying anisotropic impact ionization rates [14] [15] has been considered.

III. Results and Discussions

In this section, the on- and off-state performance of the IEMOSFETs with and without buried channel is presented. In addition, the variation in the device threshold voltage has been highlighted for different trap density values. Fig.2 shows the comparison of the I_D vs V_{GS} characteristics of 4H-SiC IEMOSFETs of 0.5 μm channel length. The presence of a buried channel in the creation of the channel at lower V_{GS} values. Hence, the IEMOSFET with the buried channel shows a threshold voltage (V_{th}) of 1.8V, while the device without the buried channel shows a higher V_{th} of 2.5 V. Fig.3 shows the comparison of I_D vs V_{DS} characteristics of the same structures at $V_{GS} = 18V$. However, this shows some exception to the previous graph. Although the device with buried channel (BC) becomes ON at much lower gate voltage, the transconductance reduces towards higher gate voltage values. Hence, at $V_{GS} = 18V$, the drain current for the buried channel MOSFET is lower than the MOSFET without buried channel.

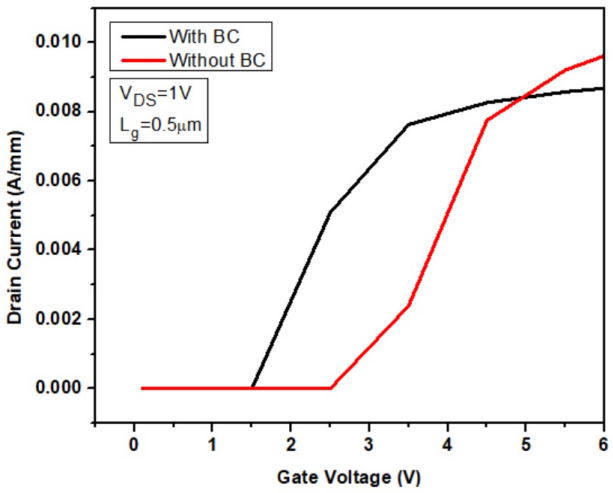

Fig. 2. Comparison of transfer characteristics of the 4H-SiC IEMOSFETs with and without BC.

Based on the output characteristics, the $R_{DS(on)}$ values have been calculated for a die area of 4X4mm^2 assuming

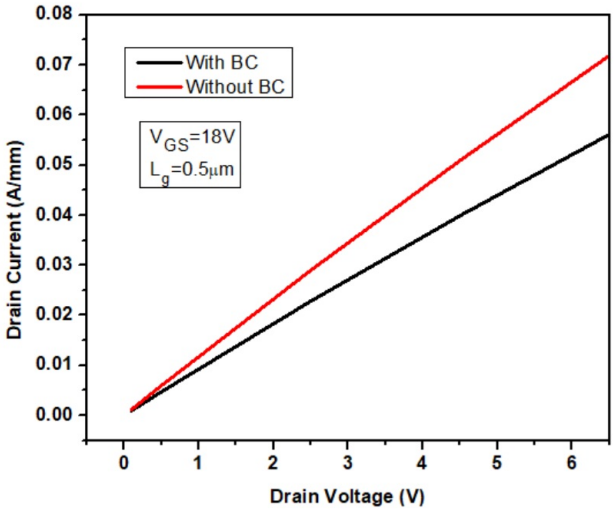

Fig. 3. Output characteristics comparison for the 4H-SiC IEMOSFETs with and without BC.

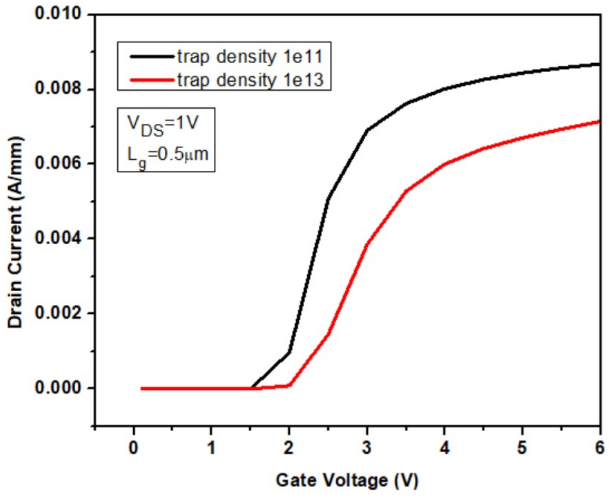

Fig. 4. Comparison of transfer characteristics for different trap densities

drain current of 40A, which is presented in Table 1. Fig.4

TABLE I

COMPARISON OF ON-RESISTANCE

Structure	Current	$R_{DS(on)}$	V_{GS}
With BC	40 A	75 mΩ	18 V
Without BC	40 A	50 mΩ	18 V

and Fig.5 show the effect of interface trap density on device performance. Simulations have been performed for two trap density values of $10^{11}cm^{-2}eV^{-1}$ and $10^{13}cm^{-2}eV^{-1}$. The degradation of mobility due to the interface trap charges as mentioned in equation 3 is reflected in the characteristics of the device. In addition, the device threshold voltage has increased for the higher trap density value $10^{13}cm^{-2}eV^{-1}$. This can be attributed to the Coulomb scattering mechanism as a result of interface trap charges, which reduce the channel carrier mobility. In addition, a comparison of the output characteristics is shown in Fig.5 for with and without buried channel designs for different trap densities. The degradation in the ON current due to interface traps is visible for higher drain current values.

Table II displays the simulated $R_{DS(on)}$ values for cases with and without buried channels and for high and low trap densities.

TABLE II

SIMULATED $R_{DS(on)}$ VALUES FOR WITH AND WITHOUT BURIED CHANNEL CASES UNDER DIFFERENT TRAP DENSITIES

Structure	I_D (A)	V_{GS} (V)	Trap Density	$R_{DS(on)}$
With BC	40	18	Low	75 mΩ
With BC	40	18	High	85 mΩ
Without BC	40	18	Low	50 mΩ
Without BC	40	18	High	60 mΩ

Comparing the minimum specific on-resistance $R_{DS(on),sp}$ value of 8mΩcm^2 for the IEMOSFETs

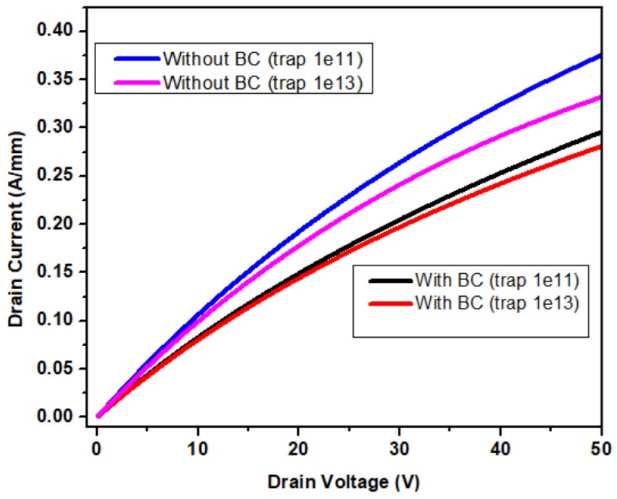

Fig. 5. Output characteristics comparison with different interface trap densities.

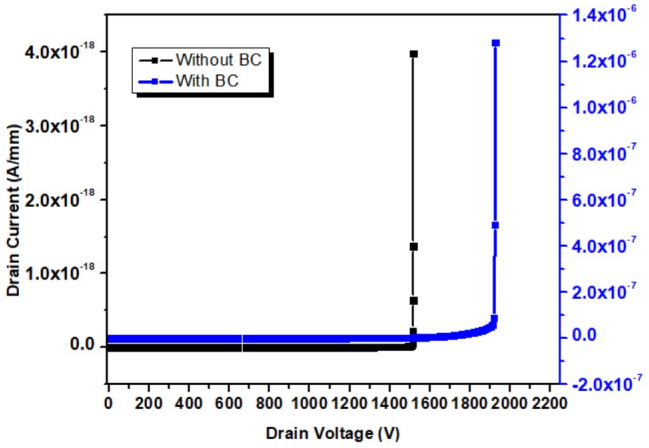

Fig. 6. Off-state breakdown characteristics for the 4H-SiC IEMOSFET designs.

(as calculated from Table II for a die area of $16mm^2$) with recently reported values of 5.8mΩcm^2 for 1.7kV modern trench gate 4H-SiC MOSFETs [16], the results are justified considering the design and fabrication complexity involved in each of these technologies.

In order to investigate the switching performance of the 4H-SiC IEMOSFETs, simulation has been performed to calculate the gate to drain parasitic capacitance as a function of V_{GS} and V_{DS}. The peak capacitance obtained per finger (length $10\mu m$) is $0.14nF$ as the drain voltage varies from $0V$ to $25V$ which is significantly lower than reported results [17].

Fig.6 shows the off-state breakdown voltage for both device structures. In the device with BC, the breakdown behavior starts at nearly 1900V whereas in the IEMOSFET without BC, it starts at around 1500V. The physical mechanism for this difference in breakdown voltages is the modulation of the punch-through effect through the p-epi layer. By performing multi-variable optimization of the device parameters (like the implant layer or epi layer thickness and doping), it was found that the above results correspond to highly optimized devices with very limited design spaces for power electronic applications in the specific 1.5-1.9 kV range.

IV. Conclusion

The on-state and off-state performances have been compared for 4H-SiC implantation-Epitaxial MOSFETs with and without a buried channel with $0.5\ \mu m$ gate length. The structure without buried channel shows a relatively higher threshold voltage, but provides lower on-resistance ($R_{DS(on)}$) at higher gate voltages. Hence, this can be a preferred choice for high voltage applications. The $R_{DS(on)}$ values are significantly modulated by interface trap density for the with-buried-channel design. Even for the without-buried-channel design, the $R_{DS(on)}$ is lower at lower trap densities. The threshold voltage of the device increases with an increase in the density of the interface traps. The degradation of mobility due to traps, which is reflected in the device output characteristics, manifests itself more strongly at higher drain voltages. An on-state current density of $2.5Amps/mm^2$ is achievable with a 80W power dissipation per $16mm^2$ die area. The technology offers the potential to increase on-state current density to $8Amps/mm^2$ with a 250W power dissipation over the same area, while keeping below the safe limits for thermal management.A comparison of the breakdown characteristics shows a breakdown of 1.9kV with buried channel and 1.5kV without buried channel.

References

[1] A. Bolotnikov, P. Losee, A. Permuy, G. Dunne, S. Kennerly, B. Rowden, J. Nasadoski, M. Harfman-Todorovic, R. Raju, F. Tao, P. Cioffi, F. J. Mueller, and L. Stevanovic, "Overview of 1.2kV-2.2kV SiC MOSFETs targeted for industrial power conversion applications," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*. Charlotte, NC, USA: IEEE, Mar. 2015, pp. 2445–2452. [Online]. Available: http://ieeexplore.ieee.org/document/7104691/

[2] C. Scognamillo, A. P. Catalano, V. D'Alessandro, M. Riccio, A. Borghese, L. Maresca, A. Irace, G. Breglio, M. Rahimo, I. Nistor, M. Antoniou, K. Melnyk, and N. Lophitis, "TCAD-Based Investigation of a 3.3 kV Planar SiC MOSFET: BV-R_{on} Trade-Off Optimization," in *2024 IEEE 18th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*. Gdynia, Poland: IEEE, June 2024, pp. 1–4. [Online]. Available: https://ieeexplore.ieee.org/document/10604369/

[3] H. Dixit, D. J. Lichtenwalner, A. Scholze, J. Kim, K. J. Han, and S. H. Ryu, "Revised Channel Mobility Model for Predictive TCAD Simulations of 4H-SiC MOSFETs," *Solid State Phenomena*, vol. 358, pp. 103–107, Aug. 2024. [Online]. Available: https://www.scientific.net/SSP.358.103

[4] S. Harada, M. Kato, M. Okamoto, T. Yatsuo, K. Fukuda, and K. Arai, "4.3 mΩcm^2, 1100 V 4H-SiC Implantation and Epitaxial MOSFET," *Materials Science Forum*, vol. 527-529, pp. 1281–1284, Oct. 2006. [Online]. Available: https://www.scientific.net/MSF.527-529.1281

[5] H. Shiomi, H. Kitai, H. Tamaso, and K. Fukuda, "Development of a novel 1200-V-class 4H-SiC implantation-and-epitaxial trench MOSFET with low on-resistance," *Japanese Journal of Applied Physics*, vol. 55, no. 4S, p. 04ER06, Apr. 2016. [Online]. Available: https://iopscience.iop.org/article/10.7567/JJAP.55.04ER06

[6] T. Tsuji, H. Shiomi, N. Ohse, Y. Onishi, and K. Fukuda, "3300V-Class 4H SiC Implantation-Epitaxial Mosfets with Low Specific On-Resistance of 11.6mΩcm^2 and High Avalanche Withstanding Capability," *Materials Science Forum*, vol. 858, pp. 962–965, May 2016. [Online]. Available: https://www.scientific.net/MSF.858.962

[7] D. Kim, N. Yun, A. J. Morgan, and W. Sung, "The Effect of Deep JFET and P-Well Implant of 1.2kV 4H-SiC MOSFETs," *IEEE Journal of the Electron Devices Society*, vol. 10, pp. 989–995, 2022. [Online]. Available: https://ieeexplore.ieee.org/document/9935108/

[8] M. Cabello, V. Soler, G. Rius, J. Montserrat, J. Rebollo, and P. Godignon, "Advanced processing for mobility improvement in 4H-SiC mosfets: A review," *Materials Science in Semiconductor Processing*, vol. 78, pp. 22–31, 2018, wide band gap semiconductors technology for next generation of energy efficient power electronics. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1369800117318978

[9] E. Brzozowski, M. Kaminski, A. Taube, O. Sadowski, K. Krol, and M. Guziewicz, "Carrier Trap Density Reduction at SiO2/4H-Silicon Carbide Interface with Annealing Processes in Phosphoryl Chloride and Nitride Oxide Atmospheres," *Materials*, vol. 16, no. 12, p. 4381, June 2023. [Online]. Available: https://www.mdpi.com/1996-1944/16/12/4381

[10] B.-Y. Tsui, Y.-T. Huang, T.-L. Wu, and C.-H. Chien, "Time-dependent dielectric breakdown of gate oxide on 4H-SiC with different oxidation processes," *Microelectronics Reliability*, vol. 123, p. 114186, Aug. 2021. [Online]. Available: https://linkinghub.elsevier.com/retrieve/pii/S0026271421001529

[11] P. Fiorenza, F. Giannazzo, M. Vivona, A. La Magna, and F. Roccaforte, "SiO2/4H-SiC interface doping during post-deposition-annealing of the oxide in N2O or POCl3," *Applied Physics Letters*, vol. 103, no. 15, p. 153508, Oct. 2013. [Online]. Available: https://pubs.aip.org/apl/article/103/15/153508/25240/SiO2-4H-SiC-interface-doping-during-post

[12] V. Uhnevionak, A. Burenkov, C. Strenger, G. Ortiz, E. Bedel-Pereira, V. Mortet, F. Cristiano, A. J. Bauer, and P. Pichler, "Comprehensive Study of the Electron Scattering Mechanisms in 4H-SiC MOSFETs," *IEEE Transactions on Electron Devices*, vol. 62, no. 8, pp. 2562–2570, Aug. 2015. [Online]. Available: https://ieeexplore.ieee.org/document/7163690/

[13] D. Klaassen, "A unified mobility model for device simulation—I. Model equations and concentration dependence," *Solid-State Electronics*, vol. 35, no. 7, pp. 953–959, July 1992. [Online]. Available: https://linkinghub.elsevier.com/retrieve/pii/0038110192903257

[14] T. Hatakeyama, "Measurements of impact ionization coefficients of electrons and holes in 4H-SiC and their application to device simulation," *physica status solidi (a)*, vol. 206, no. 10, pp. 2284–2294, Oct. 2009. [Online]. Available: https://onlinelibrary.wiley.com/doi/10.1002/pssa.200925213

[15] T. Hatakeyama, J. Nishio, C. Ota, and T. Shinohe, "Physical Modeling and Scaling Properties of 4H-SiC Power Devices," in *2005 International Conference On Simulation of Semiconductor Processes and Devices*. Tokyo, Japan: IEEE, 2005, pp. 171–174. [Online]. Available: http://ieeexplore.ieee.org/document/1562052/

[16] J.-W. Hu, K.-M. Kang, and C.-F. Huang, "A 4H-SiC 1.7 kv rated tmbs-embedded umosfet," *IEEE Electron Device Letters*, vol. 46, no. 10, pp. 1829–1832, 2025.
[17] M. Shintani, K. Oishi, Y. Nishitani, H. Takayama, and T. Sato, "Comprehensive mosfet capacitance characterization based on charge trajectories," *IEEE Transactions on Electron Devices*, vol. 72, no. 7, pp. 3758–3766, 2025.